ABSTRACT OF THE DISCLOSURE

A way predictor comprises a decoder, a memory coupled to the decoder, and a

5   circuit. The decoder is configured to decode an indication of a first address that is to

access a cache, and is configured to select a set responsive to the indication of the first

address. The memory is configured to output a plurality of values from a set of storage

locations in response to the decoder selecting the set, wherein each of the plurality of

values corresponds to a different way of the cache. Coupled to receive the plurality of

10   values and a first value corresponding to the first address, the circuit is configured to

generate a way prediction for the cache responsive to the plurality of values and the first

value.